WHAT IS CLAIMED IS

1. A chip package structure comprising:

a silicon substrate;

a die, wherein the die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of the die is adhered to the silicon substrate; and

a thin-film circuit layer located on top of the silicon substrate and the die and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die.

2. The structure in claim 1, wherein the die has an internal circuitry and a plurality of active devices located on the active surface of the die and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads.

3. The structure in claim 2, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to one of the active devices via the internal circuitry.

4. The structure in claim 3, wherein a width, length, and thickness of traces of the external circuitry are greater than corresponding traces of the internal circuitry.

5. The structure in claim 1, wherein the external circuitry further comprising a power/ground bus.

6. The structure in claim 1, wherein the thin-film circuit layer comprising at least a

patterned wiring layer and a dielectric layer, the dielectric layer is located on top of the silicon substrate and the die, and the patterned wiring layer is located on top of the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

7. The structure in claim 6, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die by the thru-holes.

8. The structure in claim 6, wherein a via is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die by the vias.

9. The structure in claim 6, wherein the patterned wiring layer and the vias form the external circuitry.

10. The structure of the claim 6, wherein the external circuitry further comprising at least one passive device.

11. The structure in claim 6, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

12. The structure in claim 10, wherein the passive device is formed by a part of the patterned wiring layer.

13. The structure in claim 6, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

14. The structure in claim 1, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the

patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the silicon substrate, the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the die through the dielectric layer that is closest to the silicon substrate, where the patterned wiring layer that is furthest away from the silicon substrate forms the bonding pads.

15. The structure in claim 14, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the die through the dielectric layer.

16. The structure in claim 15, wherein a via is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the die by the vias.

17. The structure in claim 16, wherein the patterned wiring layers and the vias form the external circuitry.

18. The structure in claim 14, wherein the external circuitry further comprising a passive device.

19. The structure in claim 18, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

20. The structure in claim 18, wherein the passive device is formed by a part of the

patterned wiring layer.

21. The structure in claim 18, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

22. The structure in claim 1, wherein the silicon substrate further comprising an inwardly protruded area located on a surface of the silicon substrate, where the backside of the die is adhered to a bottom of the inwardly protruded area.

23. The structure in claim 1, wherein the silicon substrate comprising a silicon layer and a heat conducting layer formed overlapping, a surface of the silicon substrate is a side of the heat conducting layer that is further away from the silicon layer, the silicon layer has at least one opening that penetrates through the silicon layer used to form an inwardly protruded area, and the backside of the die is adhered to a bottom of the inwardly protruded area.

24. The structure in claim 23, wherein a thickness of the silicon substrate is approximately equal to a thickness of the dies.

25. The structure in claim 1 further comprising a filling layer located between a surface of the silicon substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

26. The structure in claim 25, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

27. The structure in claim 1 further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

28. The structure in claim 1 further comprising a plurality of bonding points located

on the bonding pads.

29. The structure in claim 28, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

30. A chip package structure comprising:

a silicon substrate;

a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of each die is adhered to the silicon substrate; and

a thin-film circuit layer located on top of the silicon substrate and the die and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die.

31. The structure in claim 30, wherein the dies perform same functions.

32. The structure in claim 30, wherein the dies perform different functions.

33 The structure in claim 30, wherein the dies have an internal circuitry and a plurality of active devices located on the active surface of the die, and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads.

34. The structure in claim 33, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to one of the active devices via the internal circuitry.

35. The structure in claim 34, wherein a width, length, and thickness of traces of the

external circuitry are greater than corresponding traces of the internal circuitry.

36. The structure in claim 30, wherein the external circuitry further comprising a power/ground bus.

37. The structure in claim 30, wherein the thin-film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer is located on top of the silicon substrate and the die, and the patterned wiring layer is located on top of the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

38. The structure in claim 37, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die by the thru-holes.

39. The structure in claim 38, wherein a via is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die by the vias.

40. The structure in claim 39, wherein the patterned wiring layer and the vias form the external circuitry.

41. The structure of the claim 37, wherein the external circuitry further comprising at least one passive device.

42. The structure in claim 41, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

43. The structure in claim 41, wherein the passive device is formed by a part of the patterned wiring layer.

44. The structure in claim 37, wherein a material of the dielectric layer is selected

from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

45. The structure in claim 30, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the silicon substrate, the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the dies through the dielectric layer that is closest to the silicon substrate, where the patterned wiring layer that is furthest away from the silicon substrate forms the bonding pads.

46. The structure in claim 45, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the dies through the dielectric layer.

47. The structure in claim 46, wherein a via is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the silicon substrate is electrically connected to the metal pads of the die by the vias.

48. The structure in claim 47, wherein the patterned wiring layers and the vias form the external circuitry.

49. The structure in claim 45, wherein the external circuitry further comprising a passive device.

50. The structure in claim 49, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

51. The structure in claim 49, wherein the passive device is formed by a part of the patterned wiring layer.

52. The structure in claim 45, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

53. The structure in claim 30, wherein the silicon substrate further comprising a plurality of inwardly protruded areas located on a surface of the silicon substrate and the backside of the dies is adhered to a bottom of the inwardly protruded areas.

54. The structure in claim 30, wherein the silicon substrate comprising a silicon layer and a heat conducting layer formed thereon together, a top surface of the silicon substrate is a side of the heat conducting layer that is further away from the silicon layer, the silicon layer has a plurality of openings that penetrate through the silicon layer used to form the inwardly protruded areas, and the backside of the dies is adhered to a bottom of the inwardly protruded areas.

55. The structure in claim 54, wherein a thickness of the silicon substrate is approximately equal to a thickness of the dies.

56. The structure in claim 30 further comprising a filling layer located between a surface of the silicon substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

57. The structure in claim 56, wherein a material of the filling layer is selected from

a group consisting of epoxy and polymer.

58. The structure in claim 30 further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

59. The structure in claim 30 further comprising a plurality of bonding points located on the bonding pads.

60. The structure in claim 59, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

61. A chip packaging method comprising:

providing a silicon substrate with a surface;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of each die is adhered to the surface of the silicon substrate;

allocating a first dielectric layer on top of the surface of the silicon substrate and the active surface of the dies; and

allocating a first patterned wiring layer on top of the first dielectric layer, wherein the first patterned wiring layer is electrically connected to the metal pads of the dies through the first dielectric layer, extends to a region outside of an area above the active surfaces of the dies, and has a plurality of first bonding pads.

62. The method of claim 61, wherein the dies perform same functions.

63. The method of claim 61, wherein the dies perform different functions.

64. The method of claim 61, wherein the silicon substrate has a plurality of inwardly protruded areas located on the surface of the silicon substrate, where the backside of each die is adhered to a bottom of an inwardly protruded area.

65. The method of claim 64, wherein a depth of the inwardly protruded areas is equal

to a thickness of the dies.

66. The method of claim 64, wherein the inwardly protruded areas are formed by wet etching.

67. The method of claim 61, wherein the silicon substrate comprising a silicon layer and a heat conducting layer formed overlapping, a surface of the silicon substrate is a side of the heat conducting layer that is further away from the silicon layer, the silicon layer has a plurality of openings that penetrates through the silicon layer used to form the inwardly protruded areas, and the backside of the dies is adhered to a bottom of the inwardly protruded areas.

68. The method of claim 67, wherein the openings are formed by wet etching to remove a part of the silicon substrate until reaching the heat conducting layer.

69. The method of claim 67, wherein the heat conducting layer comprising a metal.

70. The method of claim 61, wherein after adhering the dies and before allocating the first dielectric layer, further comprising allocating a filling layer on top of the surface of the silicon substrate and surrounding the peripheral of the dies, and a top surface of the filling layer is planar to the active surface of the dies.

71. The method of claim 70, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

72. The method of claim 61, wherein after allocating the first dielectric layer and before allocating the first patterned wiring layer, further comprising patterning the first dielectric layer to form a plurality of first thru-holes that penetrates through the first dielectric layer, and the first patterned conductive is electrically connected to the metal pads of the dies by the first thru-holes.

73. The method of claim 72, wherein when allocating the first patterned wiring layer

on the first dielectric layer, further includes allocating a plurality of first vias by filling part of a conductive material of the first patterned conductive layer into the thru-holes to electrically connect the first patterned wiring layer and the metal pads of the dies by the first vias.

74. The method of claim 72, wherein when allocating the first patterned wiring layer on top of the first dielectric layer, further comprising filling the first thru-holes with a conductive material to form a plurality of first vias, by which the first patterned wiring layer and the metal pads are electrically connected.

75. The method of claim 61, wherein a material of the first dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

76. The method of claim 61, wherein the method of allocating the first patterned wiring layer on top of the first dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.

77. The method of claim 61, further comprising allocating a patterned passivation layer on top of the first dielectric layer and the first patterned wiring layer and exposing the first bonding pads.

78. The method of claim 61, further comprising allocating a bonding point on the first bonding pads.

79. The method of claim 78, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

80. The method of claim 78, further comprising singularizing the chip package structure after allocating the bonding point on the bonding pads.

81. The method of claim 80, wherein a singularization of the chip package structure

is performed on a single die.

82. The method of claim 80, wherein a singularization of the chip package structure is performed on a plurality of dies.

83. The method of claim 61 further comprising:

(a) allocating a second dielectric layer on top of the first dielectric layer and the first patterned wiring layer; and

(b) allocating a second patterned wiring layer on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads.

84. The method of claim 83, wherein after allocating the second dielectric layer and before allocating the second patterned wiring layer, further comprising patterning the second dielectric layer to form a plurality of second thru-holes, which corresponds to the first thru-holes and penetrates the second dielectric layer, to electrically connect to the first patterned wiring layer.

85. The method of claim 84, wherein when allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with part of a conductive material of the second patterned wiring layer to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.

86. The method of claim 84, wherein before allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with a conductive material to form a plurality of second vias, by which the second

patterned wiring layer is electrically connected to the first patterned wiring layer.

87. The method of claim 83, wherein a material of the second dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

88. The method of claim 83, wherein the method of allocating the second patterned wiring layer on the second dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.

89. The method of claim 83, further comprising allocating a patterned passivation layer on top of the second dielectric layer and the second patterned wiring layer and exposing the second bonding pads.

90. The method of claim 83, further comprising allocating a bonding point on the second bonding pads.

91. The method of claim 90, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

92. The method of claim 90, further comprising singularizing the chip package structure after allocating the bonding point on the second bonding pads.

93. The method of claim 92, wherein a singularization of the chip package structure is performed on a single die.

94. The method of claim 92, wherein a singularization of the chip package structure is performed on a plurality of dies.

95. The method of claim 83, further comprising repeating step (a) and step (b) a plurality of times.

96. The method of claim 95 further comprising allocating a patterned passivation layer on the second dielectric layer and the second patterned wiring layer that is furthest

away from the silicon substrate and exposing the second bonding pads of the second patterned wiring layer that is furthest away from the silicon substrate.

97. The method of claim 95, further comprising allocating a bonding point on the second bonding pads of the second dielectric layer that is furthest away from the silicon substrate.

98. The method of claim 97, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

99. The method of claim 97, further comprising singularizing the chip package structure after allocating the bonding point on the second bonding pads.

100. The method of claim 99, wherein a singularization of the chip package structure is performed on a single die.

101. The method of claim 100, wherein a singularization of the chip package structure is performed on a plurality of dies.

102. A chip packaging method comprising:

providing a substrate with a first surface;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the active surface of each die is adhered to the first surface of the substrate;

allocating a first filling layer on top of the first surface of the substrate and surrounding the dies;

planarizing and thinning of the first filling layer and the dies;

providing a silicon substrate with a second surface and adhering the second surface of the silicon substrate to the first filling layer and the dies;

removing the first filling layer and the substrate;

allocating a first dielectric layer on the second surface of the silicon substrate and the active surface of the dies; and

allocating a first patterned wiring layer on top of the first dielectric layer, wherein the first patterned wiring layer is electrically connected to the metal pads of the dies through the first dielectric layer, extends to a region outside the active surfaces of the dies, and has a plurality of first bonding pads.

103. The method of claim 102, wherein the dies perform same functions.

104. The method of claim 102, wherein the dies perform different functions.

105. The method of claim 102, wherein a material of the substrate is selected from a group consisting of glass, ceramic, silicon, and organic material.

106. The method of claim 102, wherein a material of the first filling layer is selected from a group consisting of epoxy and polymer.

107. The method of claim 102, wherein after adhering the silicon substrate and before removing the first filling layer and the substrate, further comprising allocating a second filling layer on top of the second surface of the silicon substrate, the second filling layer surrounds a peripheral of the dies and has a top surface that is planar to the active surface of the dies.

108. The method of claim 107, wherein a material of the second filling layer is selected from a group consisting of epoxy and polymer.

109. The method of claim 102, wherein after allocating the first dielectric layer and before allocating the first patterned wiring layer, further comprising patterning the first dielectric layer to form a plurality of first thru-holes, by which the first patterned wiring layer is electrically connected to the metal pads of the dies.

110. The method of claim 109, wherein when allocating the first patterned wiring layer on top of the first dielectric layer, further comprising filling the first thru-holes with part of a conductive material of the first patterned wiring layer to form a plurality of first vias, by which the first patterned wiring layer is electrically connected to the metal pads of the dies.

111. The method of claim 109, wherein before allocating the first patterned wiring layer on top of the first dielectric layer, further comprising filling the first thru-holes with a conductive material to form a plurality of first vias, by which the first patterned wiring layer is electrically connected to the metal pads of the dies.

112. The method of claim 102, wherein a material of the first dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

113. The method of claim 102, wherein a method of allocating the first patterned wiring layer on the first dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.

114. The method of claim 102, further comprising allocating a patterned passivation layer on top of the first dielectric layer and the first patterned wiring layer and exposing the first bonding pads.

115. The method of claim 102, further comprising allocating a bonding point on the first bonding pads.

116. The method of claim 115, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

117. The method of claim 115, further comprising singularizing the chip package structure after allocating the bonding point on the first bonding pads.

118. The method of claim 117, wherein a singularization of the chip package structure is performed on a single die.

119. The method of claim 117, wherein a singularization of the chip package structure is performed on a plurality of dies.

120. The method of claim 102 further comprising:

(a) allocating a second dielectric layer on top of the first dielectric layer and the first patterned wiring layer; and

(b) allocating a second patterned wiring layer on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads.

121. The method of claim 120, wherein after allocating the second dielectric layer and before allocating the second patterned wiring layer, further comprising patterning the second dielectric layer to form a plurality of second thru-holes, which corresponds to the first bonding pads and penetrates the second dielectric layer, to electrically connect to the first patterned wiring layer.

122. The method of claim 121, wherein when allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru-holes with part of a conductive material of the second patterned wiring layer to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.

123. The method of claim 121, wherein before allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second

thru-holes with a conductive material to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.

124. The method of claim 120, wherein a material of the second dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

125. The method of claim 120, wherein a method of allocating the second patterned wiring layer on the second dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.

126. The method of claim 120, further comprising allocating a patterned passivation layer on top of the second dielectric layer and the second patterned wiring layer and exposing the second bonding pads.

127. The method of claim 120, further comprising allocating a bonding point on the second bonding pads.

128. The method of claim 127, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

129. The method of claim 127, further comprising singularizing the chip package structure after allocating the bonding point on the second bonding pads.

130. The method of claim 129, wherein a singularization of the chip package structure is performed on a single die.

131. The method of claim 129, wherein a singularization of the chip package structure is performed on a plurality of dies.

132. The method of claim 120, further comprising repeating step (a) and step (b) a plurality of times.

133. The method of claim 132 further comprising allocating a patterned passivation

layer on the second dielectric layer and the second patterned wiring layer that are furthest away from the silicon substrate and exposing the second bonding pads of the second patterned wiring layer that is furthest away from the silicon substrate.

134. The method of claim 132, further comprising allocating a bonding point on the second bonding pads of the second patterned wiring layer that is furthest away from the silicon substrate.

135. The method of claim 134, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

136. The method of claim 134, further comprising singularizing the chip package structure after allocating the bonding point on the second bonding pads.

137. The method of claim 136, wherein a singularization of the chip package structure is performed on a single die.

138. The method of claim 136, wherein a singularization of the chip package structure is performed on a plurality of dies.